



# PBL2001D

20 V PNP BISS loadswitch

Rev. 01 — 5 July 2005

Product data sheet

## 1. Product profile

### 1.1 General description

PNP low  $V_{CEsat}$  Breakthrough in Small Signal (BISS) transistor and NPN Resistor-Equipped Transistor (RET) in a SOT457 (SC-74) small Surface Mounted Device (SMD) plastic package.

### 1.2 Features

- Low  $V_{CEsat}$  (BISS) and resistor-equipped transistor in one package
- Low threshold voltage (< 1 V) compared to MOSFET
- Low drive power required
- Space-saving solution
- Reduction of component count

### 1.3 Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

### 1.4 Quick reference data

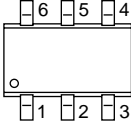
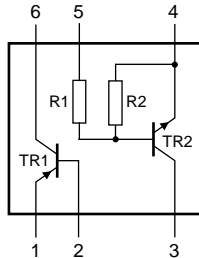
Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1; PNP low <math>V_{CEsat}</math> transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	-20	V
$I_C$	collector current (DC)		-	-	-1	A
$R_{CEsat}$	collector-emitter saturation resistance	$I_C = -1$ A; $I_B = -100$ mA	[1]	185	280	m $\Omega$
<b>TR2; NPN resistor-equipped transistor</b>						
$V_{CEO}$	collector-emitter voltage	open base	-	-	50	V
$I_O$	output current		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

[1] Pulse test:  $t_p \leq 300$   $\mu$ s;  $\delta \leq 0.02$ .

## 2. Pinning information

**Table 2: Pinning**

Pin	Description	Simplified outline	Symbol
1	emitter TR1		
2	base TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	collector TR1		

*sym036*

## 3. Ordering information

**Table 3: Ordering information**

Type number	Package		
	Name	Description	Version
PBLS2001D	SC-74	plastic surface mounted package; 6 leads	SOT457

## 4. Marking

**Table 4: Marking codes**

Type number	Marking code
PBLS2001D	F6

## 5. Limiting values

**Table 5: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

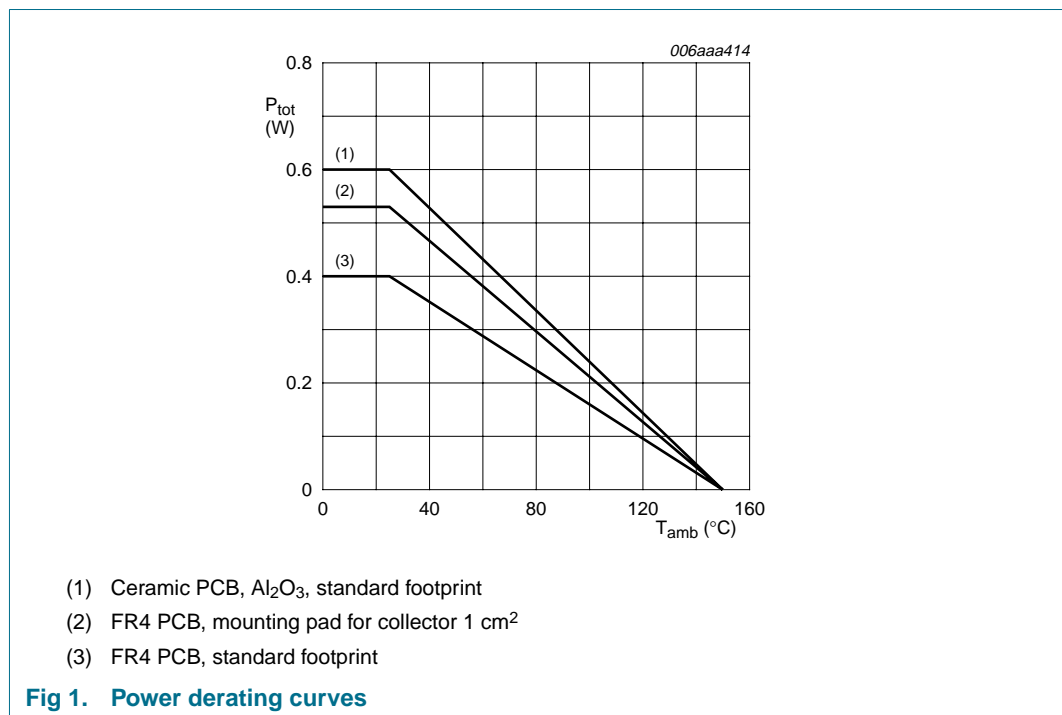
Symbol	Parameter	Conditions	Min	Max	Unit	
<b>TR1; PNP low <math>V_{CEsat}</math> transistor</b>						
$V_{CBO}$	collector-base voltage	open emitter	-	-20	V	
$V_{CEO}$	collector-emitter voltage	open base	-	-20	V	
$V_{EBO}$	emitter-base voltage	open collector	-	-5	V	
$I_C$	collector current (DC)		-	-1	A	
$I_{CM}$	peak collector current	$t_p \leq 300 \mu s$	-	-2	A	
$I_B$	base current (DC)		-	-0.3	A	
$I_{BM}$	peak base current	$t_p \leq 300 \mu s$	-	-0.6	A	
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	-	250	mW
			[2]	-	350	mW
			[3]	-	400	mW

**Table 5: Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>TR2; NPN resistor-equipped transistor</b>					
$V_{CBO}$	collector-base voltage	open emitter	-	50	V
$V_{CEO}$	collector-emitter voltage	open base	-	50	V
$V_{EBO}$	emitter-base voltage	open collector	-	10	V
$V_I$	input voltage				
	positive		-	+12	V
	negative		-	-10	V
$I_O$	output current		-	100	mA
$I_{CM}$	peak collector current	$t_p \leq 300 \mu s$	-	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$	[1]	-	200 mW
<b>Per device</b>					
$P_{tot}$	total power dissipation		[1]	-	400 mW
			[2]	-	530 mW
			[3]	-	600 mW
$T_{stg}$	storage temperature		-65	+150	$^\circ\text{C}$
$T_j$	junction temperature		-	150	$^\circ\text{C}$
$T_{amb}$	ambient temperature		-65	+150	$^\circ\text{C}$

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.

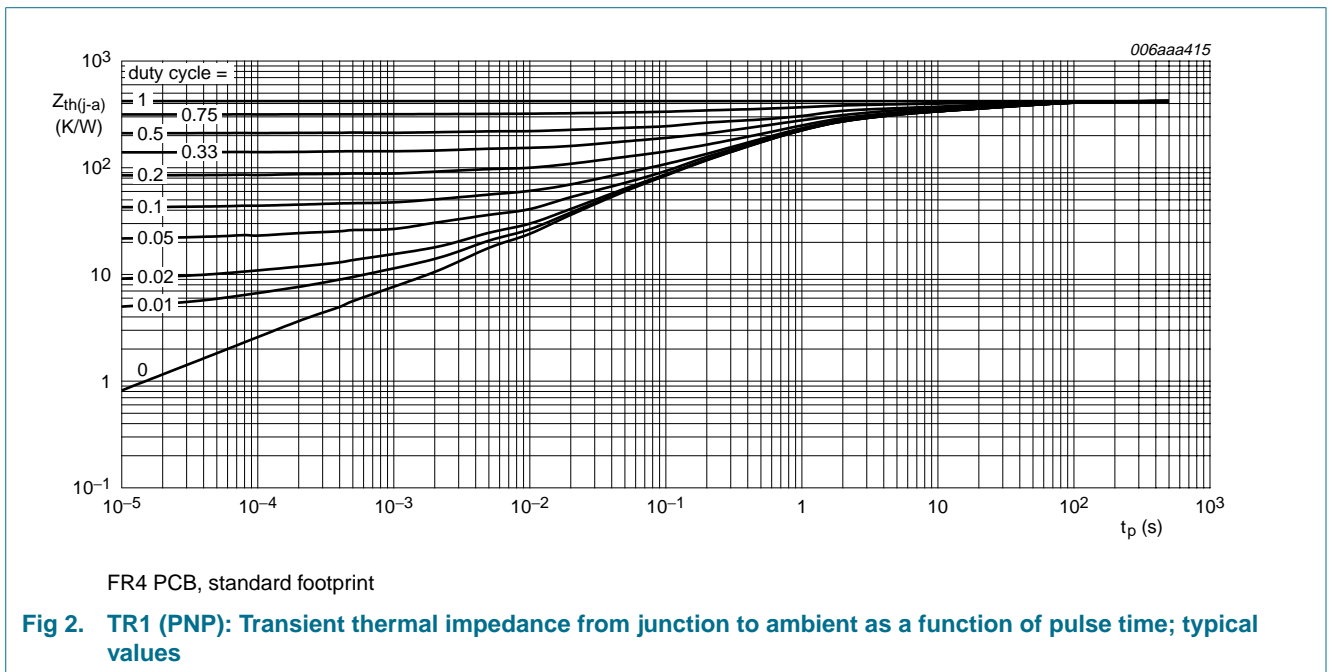


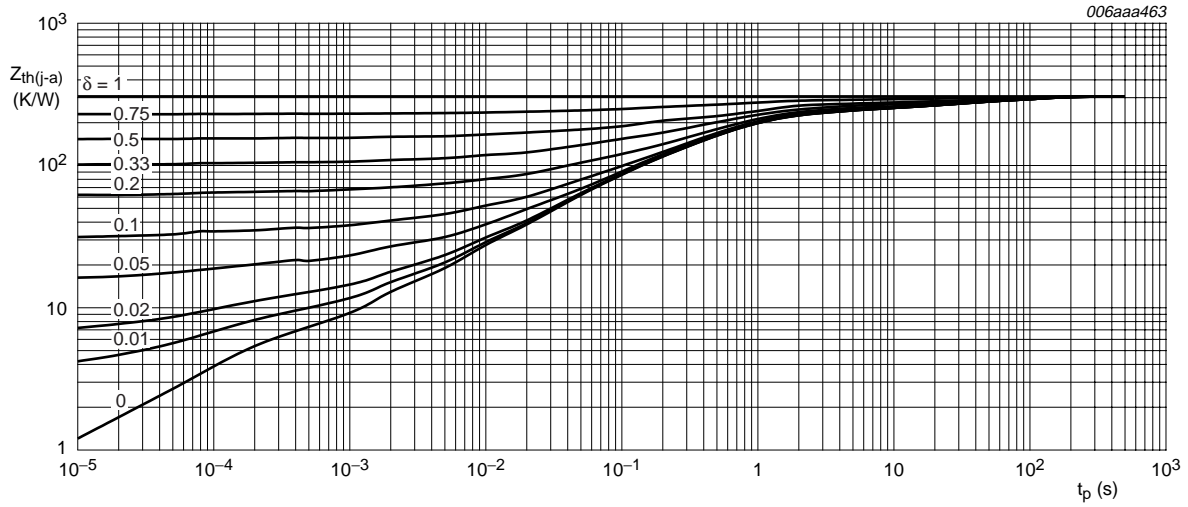
## 6. Thermal characteristics

**Table 6: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	315	K/W
			[2]	-	-	236	K/W
			[3]	-	-	210	K/W

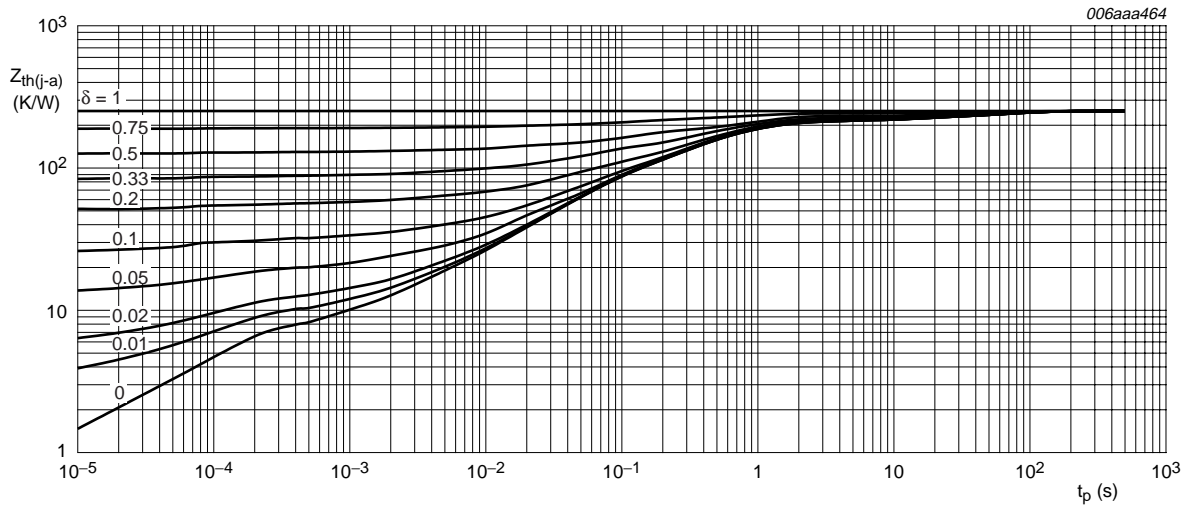
- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm<sup>2</sup>.
- [3] Device mounted on a ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint.





FR4 PCB, mounting pad for collector 1 cm<sup>2</sup>

**Fig 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values**



Ceramic PCB, Al<sub>2</sub>O<sub>3</sub>, standard footprint

**Fig 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse time; typical values**

## 7. Characteristics

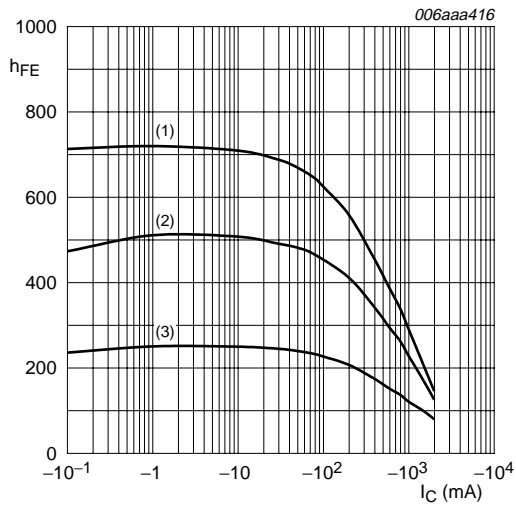
**Table 7: Characteristics**
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>TR1; PNP low V<sub>CEsat</sub> transistor</b>							
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -20 V; I <sub>E</sub> = 0 A	-	-	-0.1	μA	
		V <sub>CB</sub> = -20 V; I <sub>E</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	μA	
I <sub>CES</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -20 V; V <sub>BE</sub> = 0 V	-	-	-0.1	μA	
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-0.1	μA	
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -2 V; I <sub>C</sub> = -1 mA	220	495	-		
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -100 mA	220	440	-		
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -500 mA	[1]	220	310	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -1 A	[1]	155	220	-	
		V <sub>CE</sub> = -2 V; I <sub>C</sub> = -2 A	[1]	60	120	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -100 mA; I <sub>B</sub> = -1 mA	-	-55	-90	mV	
		I <sub>C</sub> = -500 mA; I <sub>B</sub> = -50 mA	[1]	-	-100	-150	mV
		I <sub>C</sub> = -1 A; I <sub>B</sub> = -50 mA	[1]	-	-200	-300	mV
		I <sub>C</sub> = -1 A; I <sub>B</sub> = -100 mA	[1]	-	-185	-280	mV
R <sub>CEsat</sub>	collector-emitter saturation resistance	I <sub>C</sub> = -1 A; I <sub>B</sub> = -100 mA	[1]	-	185	280	mΩ
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = -1 A; I <sub>B</sub> = -50 mA	[1]	-	-0.95	-1.1	V
		I <sub>C</sub> = -1 A; I <sub>B</sub> = -100 mA	[1]	-	-1	-1.1	V
V <sub>BEon</sub>	base-emitter turn-on voltage	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -1 A	[1]	-	-0.85	-1.1	V
t <sub>d</sub>	delay time	I <sub>C</sub> = -1 A; I <sub>Bon</sub> = -50 mA;	-	8	-	ns	
t <sub>r</sub>	rise time	I <sub>Boff</sub> = 50 mA	-	34	-	ns	
t <sub>on</sub>	turn-on time		-	42	-	ns	
t <sub>s</sub>	storage time		-	140	-	ns	
t <sub>f</sub>	fall time		-	45	-	ns	
t <sub>off</sub>	turn-off time		-	185	-	ns	
f <sub>T</sub>	transition frequency	I <sub>C</sub> = -50 mA; V <sub>CE</sub> = -10 V; f = 100 MHz	150	185	-	MHz	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz	-	15	20	pF	

**Table 7: Characteristics ...continued** $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

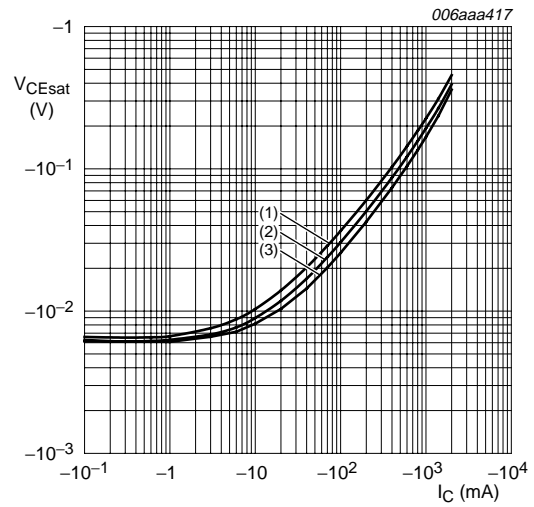
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR2; NPN resistor-equipped transistor</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	$\mu\text{A}$
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	2	mA
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 20\text{ mA}$	30	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	-	1.2	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 20\text{ mA}$	2	1.6	-	V
R1	bias resistor 1 (input)		1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	2.5	pF

[1] Pulse test:  $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$ .



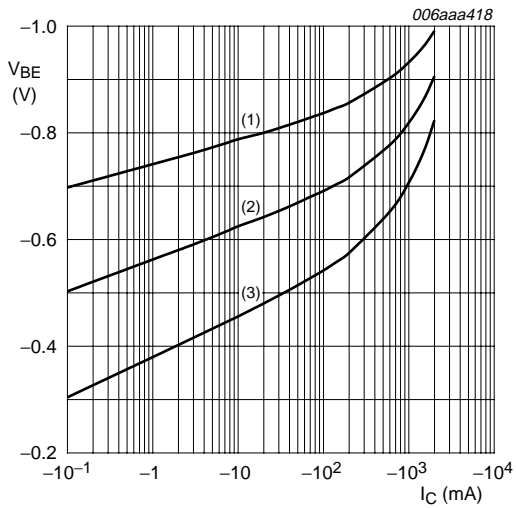
$V_{CE} = -2\text{ V}$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig 5. TR1 (PNP): DC current gain as a function of collector current; typical values**



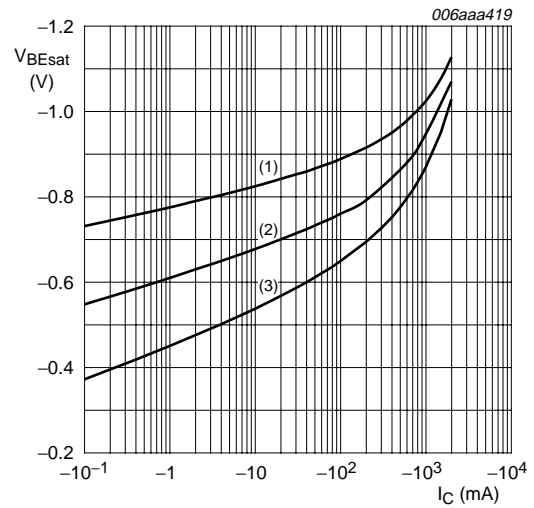
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -55\text{ }^\circ\text{C}$

**Fig 6. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = -5\text{ V}$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

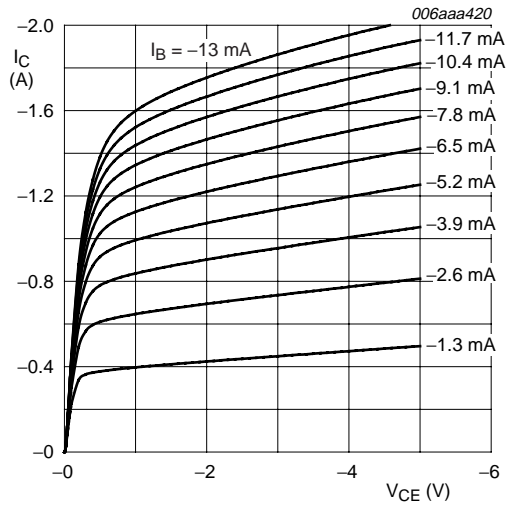
**Fig 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values**



$I_C/I_B = 20$   
 (1)  $T_{amb} = -55\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

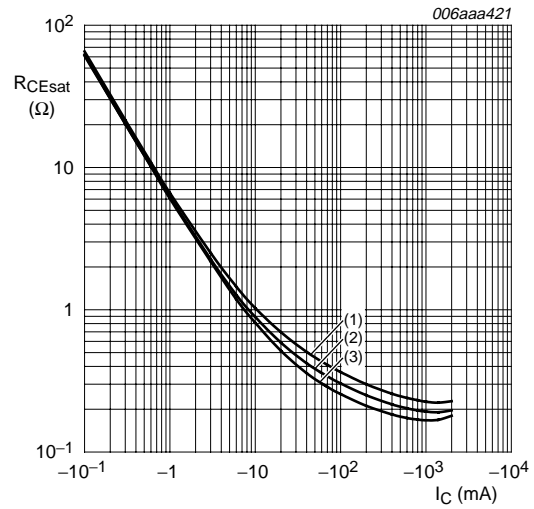
**Fig 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values**





$T_{amb} = 25$  °C

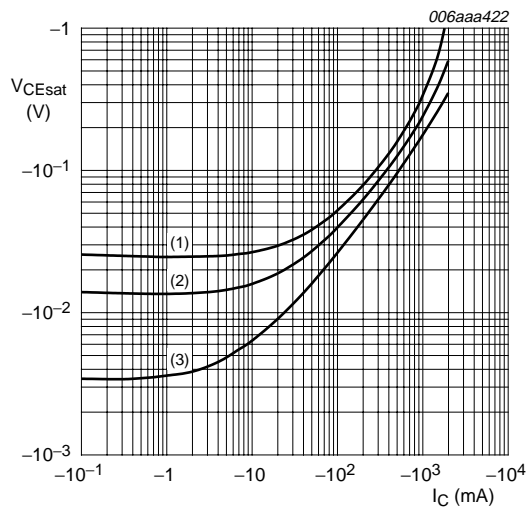
Fig 9. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values



$I_C/I_B = 20$

- (1)  $T_{amb} = 100$  °C
- (2)  $T_{amb} = 25$  °C
- (3)  $T_{amb} = -55$  °C

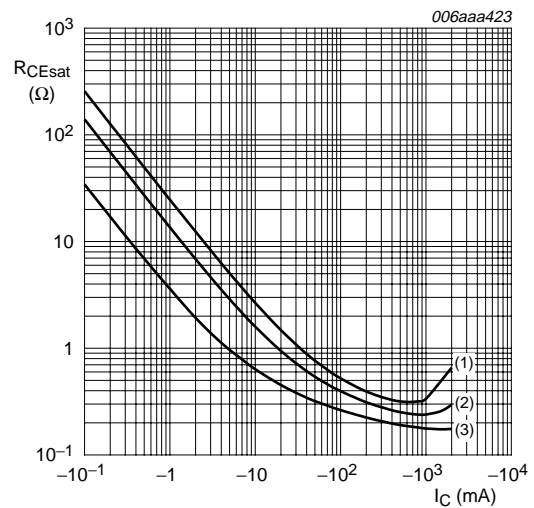
Fig 10. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25$  °C

- (1)  $I_C/I_B = 100$
- (2)  $I_C/I_B = 50$
- (3)  $I_C/I_B = 10$

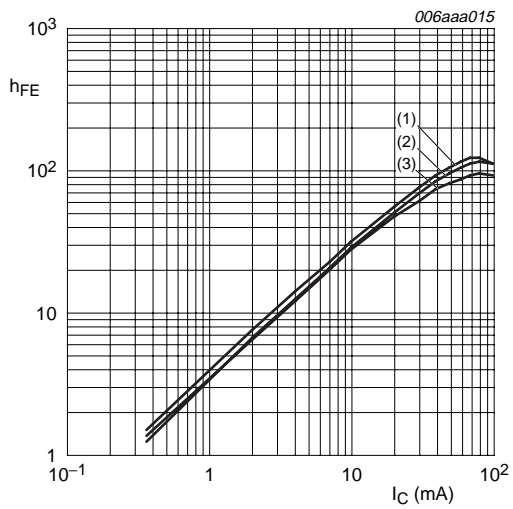
Fig 11. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



$T_{amb} = 25$  °C

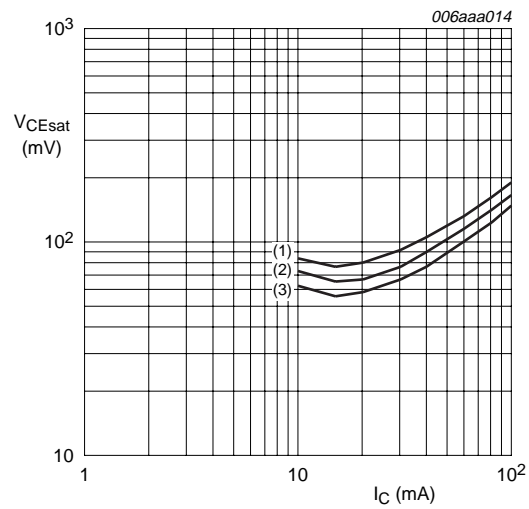
- (1)  $I_C/I_B = 100$
- (2)  $I_C/I_B = 50$
- (3)  $I_C/I_B = 10$

Fig 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



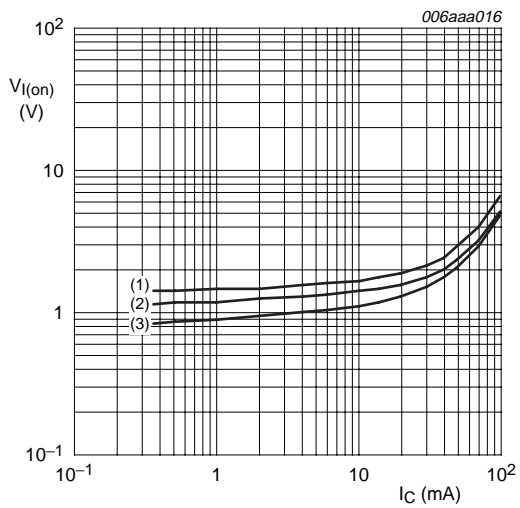
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = 150\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig 13. TR2 (NPN): DC current gain as a function of collector current; typical values**



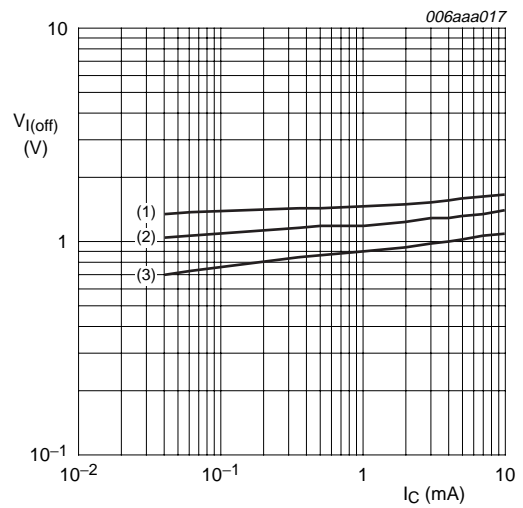
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig 14. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = 0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

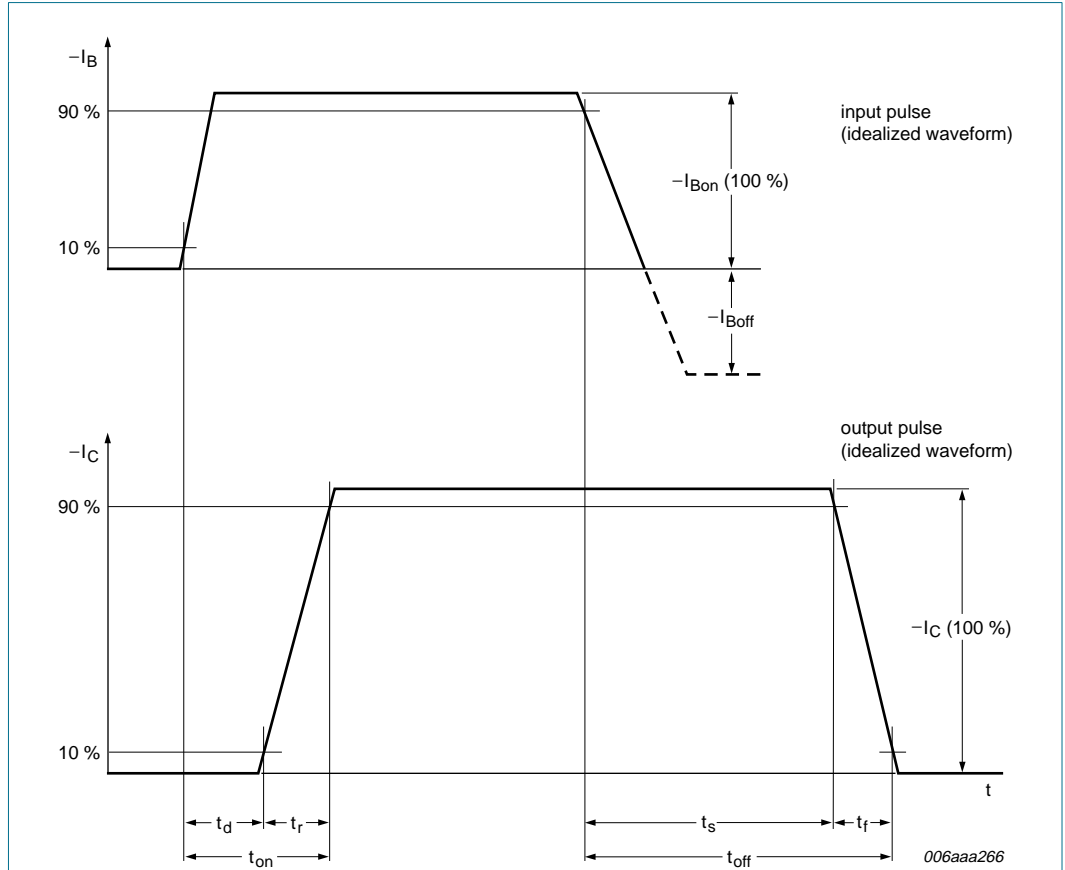
**Fig 15. TR2 (NPN): On-state input voltage as a function of collector current; typical values**



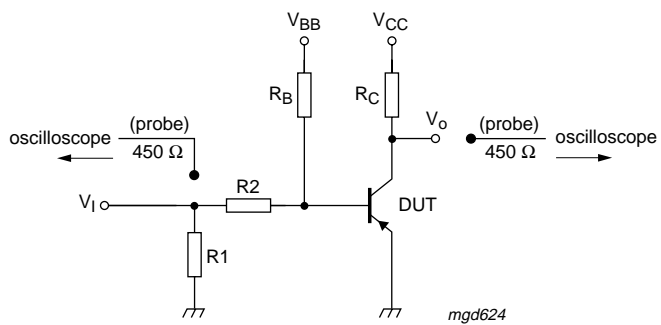
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig 16. TR2 (NPN): Off-state input voltage as a function of collector current; typical values**

**8. Test information**



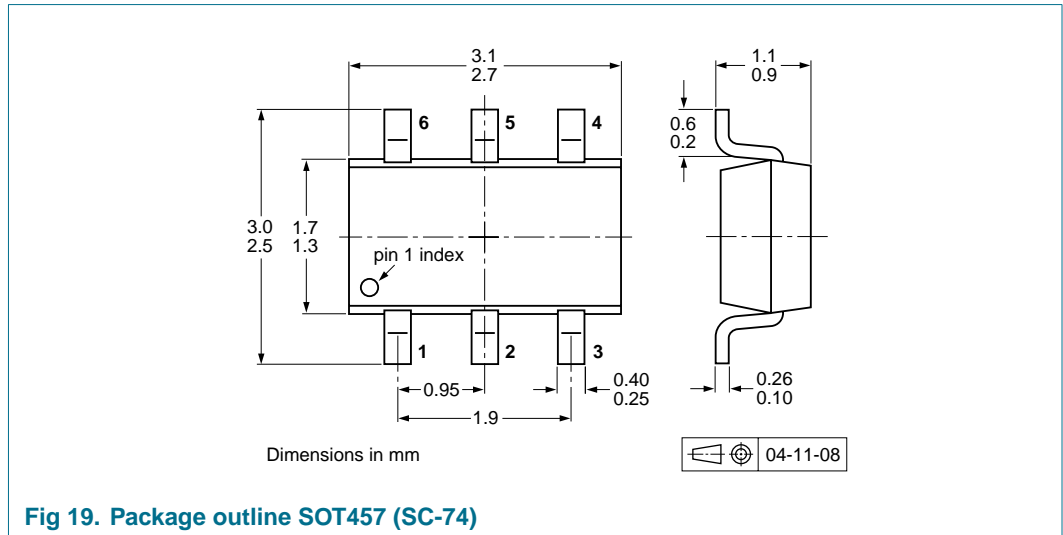
**Fig 17. BISS transistor switching time definition**



$I_C = -1$  A;  $I_{Bon} = -50$  mA;  $I_{Boff} = 50$  mA;  $R_1 = \text{open}$ ;  $R_2 = 45$   $\Omega$ ;  $R_B = 145$   $\Omega$ ;  $R_C = 10$   $\Omega$

**Fig 18. Test circuit for switching times**

## 9. Package outline



## 10. Packing information

**Table 8: Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code. [\[1\]](#)

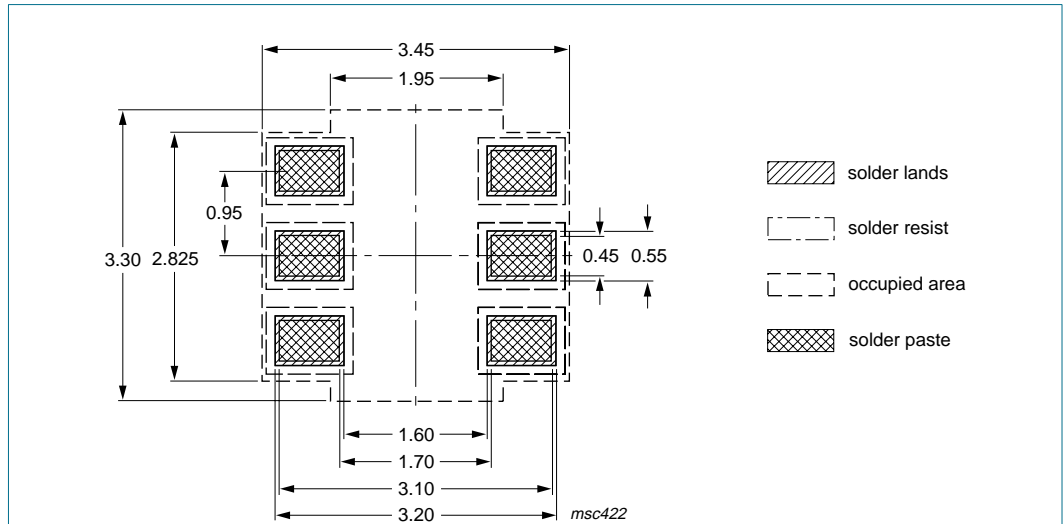
Type number	Package	Description	Packing quantity	
			3000	10000
PBLS2001D	SOT457	4 mm pitch, 8 mm tape and reel; T1	<a href="#">[2]</a> -115	-135
		4 mm pitch, 8 mm tape and reel; T2	<a href="#">[3]</a> -125	-165

[1] For further information and the availability of packing methods, see [Section 17](#).

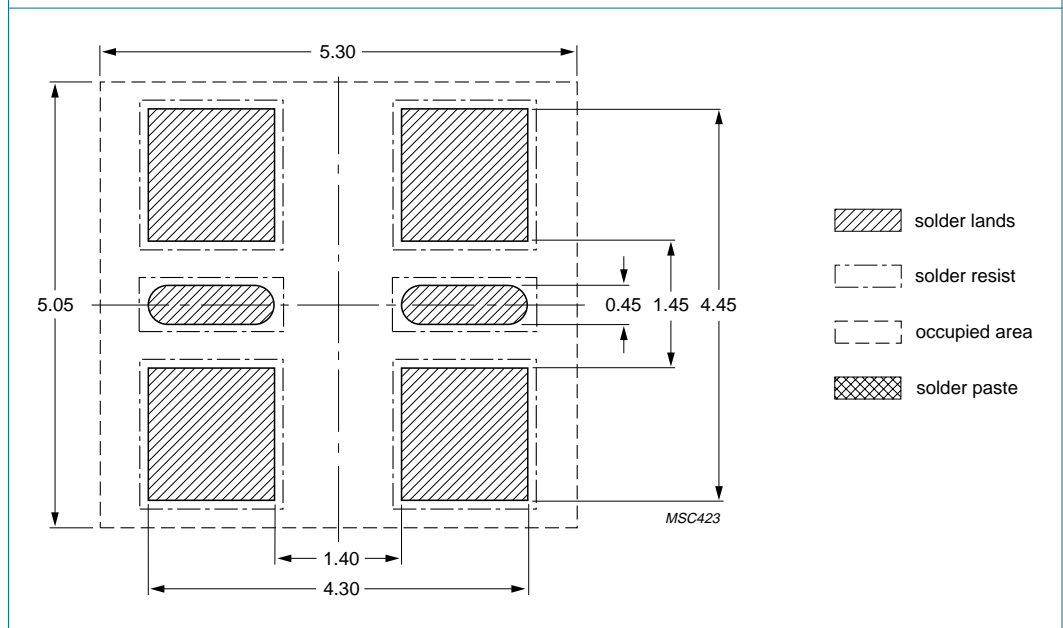
[2] T1: normal taping

[3] T2: reverse taping

**11. Soldering**



**Fig 20. Reflow soldering footprint**



**Fig 21. Wave soldering footprint**



## 12. Revision history

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**Table 9: Revision history**

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PBLS2001D_1	20050705	Product data sheet	-	-	-

## 13. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 14. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 15. Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

## 17. Contact information

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## 18. Contents

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